Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers respectively formed in the source region and the drain region, and which are in contact with the channel region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of metallic silicide layers extend to bottom surfaces of the semiconductor layer,

wherein the metallic silicide layers are composed of refractory metal and silicon, ~~wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:~~

~~(X / Y) > (X0 / Y0), and~~

wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than 1×10^{-7} Ω - cm^2, and

wherein the semiconductor layer has a thickness of 20 nm.

Claim 2 (Previously Presented): The field effect transistor according to claim 1, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

Claim 3 (Previously Presented): A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers respectively formed in the source region and the drain region, and which are in contact with the channel region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of cobalt silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

Claim 4 (Previously Presented): The field effect transistor according to claim 3, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

Claim 5 (Currently Amended): A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;

a pair of impurity layers respectively formed in the source region and the drain region, and which are in contact with the channel region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from an upper surface of the metallic silicide layers to a bottom surface of the semiconductor layer,

wherein the metallic silicide layers are composed of refractory metal and silicon, ~~wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:~~

~~(X / Y) > (X0 / Y0), and~~

wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than 1×10^{-7} Ω - cm^2, and

wherein the semiconductor layer has a thickness of 20 nm.

Claim 6 (Previously Presented): The field effect transistor according to claim 5, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

Claim 7 (Previously Presented): A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers respectively formed in the source region and the drain region, and which are in contact with the channel region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of cobalt silicide layers have a thickness which is equal to or more than 80% thickness of from an upper surface of the cobalt silicide layers to a bottom surface of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

Claim 8 (Previously Presented): The field effect transistor according to claim 7, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

Claim 9 (Currently Amended): A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first impurity layer and the first metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second impurity layer and the second metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer,

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is between the first impurity layer and the second impurity layer,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon,

~~wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:~~

~~(X / Y) > (X0 / Y0), and~~

wherein a first contact specific resistance between the first metallic silicide layer and the first impurity layer, and a second contact specific resistance between the second metallic silicide layer and the second impurity layer, are less than 1×10^{-7} Ω - cm^2, and

wherein the semiconductor layer has a thickness of 20 nm.

Claim 10 (Previously Presented): The field effect transistor according to claim 9, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

Claim 11 (Previously Presented): A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first impurity layer and the first cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second impurity layer and the second cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is between the first impurity layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

Claim 12 (Previously Presented): The field effect transistor according to claim 11, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

Claim 13 (Currently Amended): A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first metallic silicide layer has a thickness which is equal to or more than 80% a thickness of from an upper surface of the first metallic silicide layer to a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second metallic silicide layer has a thickness which is equal to or more than 80% a thickness of from an upper surface of the second metallic silicide layer to a bottom surface of the semiconductor layer,

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is between the first impurity layer and the second impurity layer,

wherein the first metallic silicide layer and the second metallic silicide layer are

composed of refractory metal and silicon,

~~wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:~~

~~(X / Y) > (X0 / Y0), and~~

wherein a first contact specific resistance between the first metallic silicide layer and the first impurity layer, and a second contact specific resistance between the second metallic silicide layer and the second impurity layer, are less than 1×10^{-7} Ω - cm^2, and

wherein the semiconductor layer has a thickness of 20 nm.

Claim 14 (Previously Presented): The field effect transistor according to claim 13, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

Claim 15 (Previously Presented): A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first cobalt silicide layer has a thickness which is equal to or more than 80% thickness of from an upper surface of the first cobalt silicide layer to a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second cobalt silicide layer has a thickness which is equal to or more than 80% thickness of from an upper surface of the second cobalt silicide layer to a bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is between the first impurity layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

Claim 16 (Previously Presented): The field effect transistor according to claim 15, wherein said field effect transistor has a depletion layer which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to a gate electrode thereof.

Claims 17-23 (Canceled)

Claim 24 (Previously Presented): The field effect transistor according to claim 3, wherein a contact specific resistance between the cobalt silicide layers and the impurity layers is less than 1×10^{-7} Ω - cm^2.

Claim 25 (Canceled)

Claim 26 (Previously Presented): The field effect transistor according to claim 7, wherein a contact specific resistance between the cobalt silicide layers and the impurity layers is less than 1×10^{-7} Ω - cm^2.

Claim 27 (Canceled)

Claim 28 (Previously Presented): The field effect transistor according to claim 11, wherein a first contact specific resistance between the first cobalt silicide layer and the first impurity layer, and a second contact specific resistance between the second cobalt silicide layer and the second impurity layer, are less than 1×10^{-7} Ω - cm^2.

Claim 29 (Canceled)

Claim 30 (Previously Presented): The field effect transistor according to claim 15, wherein a first contact specific resistance between the first cobalt silicide layer and the

first impurity layer, and a second contact specific resistance between the second cobalt silicide layer and the second impurity layer, are less than 1×10^{-7} Ω - cm^2.

Claim 31 (Previously Presented): The field effect transistor according to claim 5, wherein the pair of impurity layers respectively extend between the pair of metallic silicide layers and the bottom surface of the semiconductor layer.

Claim 32 (Previously Presented): The field effect transistor according to claim 7, wherein the pair of impurity layers respectively extend between the pair of cobalt silicide layers and the bottom surface of the semiconductor layer.

Claim 33 (Previously Presented): The field effect transistor according to claim 13, wherein the first impurity layer extends between the first metallic silicide layer and the bottom surface of the semiconductor layer, and wherein the second impurity layer extends between the second metallic silicide layer and the bottom surface of the semiconductor layer.

Claim 34 (Previously Presented): The field effect transistor according to claim 15, wherein the first impurity layer extends between the first cobalt silicide layer and the bottom surface of the semiconductor layer, and wherein the second impurity layer extends between the second cobalt silicide layer and the bottom surface of the

semiconductor layer.